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Docket No.: GR 00 P 1281

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By: _____ Date: 4/10/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Harald Bachhofer et al.
Applic. No.	:	09/783,187
Filed	:	February 14, 2001
Title	:	Memory Configuration And Method For Reading A State From And Storing A State In A Ferroelectric Transistor

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,946,224 (Nishimura), dated August 31, 1999;

Takashi Nakamura et al.: "A Single-Transistor Ferroelectric Memory Cell", 1995 IEEE International Solid-State Circuits Conference, pp. 68-69;

Jong-Son Lyu et al.: "Metal-Ferroelectric-Semiconductor Field-Effect Transistor (MFSFET) for Single Transistor Memory by Using Poly-Si Source/Drain and a $BaMgF_4$ Dieelectric", IEDM 1996, pp. 503-506.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications,

patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

Mark P. Weichselbaum
Reg. No. 43,248

For Applicants

Date: April 10, 2001

Lerner And Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

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